

ADC and DAC Converters

ONE-MARK QUESTIONS

- 10.1** It is given that a minimum to a maximum in 100 increments are required. It means we need to find out $(100)_d = (...?)_b$. i.e., $(100)_d = (110\ 0100)_b$. So, 7 bits are required and option 'd' is correct.
- 10.2** Number of comparators required to build N bit flash ADC = $2^N - 1$. Therefore, 255 comparators will be required to build an 8-bit flash ADC and option 'c' is correct.
- 10.3** The number of comparators required in a N-bit comparator type ADC is = $2^N - 1$. So, 7 comparators will be required in a 3-bit comparator type ADC and hence option 'c' is correct.
- 10.4** A successive approximation analogue to digital converter requires N clock pulses to convert a N bit number. However, in this example 8 bits are used to represent voltages up to full scale reading i.e. 2.55 V. So, the conversion time required for 2 V will be 20 μ s and option 'b' is correct.
- 10.5** Number of comparators required to build N bit flash ADC = $2^N - 1$. Therefore, 15 comparators will be required to build a 4-bit flash ADC and option 'c' is correct.

TWO-MARKS QUESTIONS

- 10.1** Number of comparators required to in N bit flash ADC = $2^N - 1$. Here, N = 8 is given and hence 255 comparators will be required. But the input capacitance of each comparator is 8 pF. We know that in flash ADC all comparators are connected in parallel. So, the total input capacitance = $255 \times 8\text{ pF} = 2.04\text{ nF}$ and the input RC time constant of the circuit is $\tau = RC = 75\Omega \times 2.04\text{ nF} = 153\text{ nS}$. It is expected that the input must settle within 0.5 LSB which is $= \frac{1}{2} \times \frac{1}{2^{N-1}} V_{in} = \frac{1}{2} \times \frac{1}{255} V_{in} = \frac{V_{in}}{510}$. Therefore, voltage across the capacitor must settle to

$$V_c = V_{in} - \frac{V_{in}}{510} = \frac{509}{510} V_{in} \dots \dots \dots (1)$$

Now calculating voltage across capacitor using below relationship

$$V_c(t) = V_{\infty} + (V_0 - V_{\infty})e^{-\frac{t}{\tau}}$$

We know $V_{\infty} = V_{in}$ and $V_0 = 0$. Now substituting these values we can write

$$V_c(t) = V_{in} + (0 - V_{in})e^{-\frac{t}{\tau}}$$

$$\therefore V_c(t) = V_{in} \left(1 + e^{-\frac{t}{\tau}}\right) \dots \dots \dots (2)$$

Now equating (1) and (2) $\therefore V_c(t) = V_{in} \left(1 + e^{-\frac{t}{\tau}}\right) = \frac{509}{510} V_{in}$

$$\therefore \left(1 + e^{-\frac{t}{\tau}}\right) = \frac{509}{510}$$

$$t = -\tau \cdot \ln \left(1 - \frac{509}{510}\right) = 953.87\text{ nS}$$

So, 953.87 nS will be required for the input to settle to an accuracy of 0.5 LSB even for a full scale input change for proper conversion and hence sampling rate required is $f_{sample} = \frac{1}{953.87nS} = 1.05 \text{ M samples}$ and the closest answer is 1 mega samples per second which is option 'a'.

- 10.2** It is clear from the given data that the resolution of the ADC is 0.0625V. There are 15 such steps. So, $0.0625 \times 15 = 0.9375V$. So, the correct answer can be 0.93 to 0.94v.

- 10.3** The relation between counter output and DAC output is given as

$$V_{DAC} = \sum_{n=0}^3 2^{n-1} b_n = 2^2 b_3 + 2^1 b_2 + 2^0 b_1 + 2^{-1} b_0 = 4b_3 + 2b_2 + 1b_1 + 0.5b_0$$

If we substitute counter output = 0001 in the above expression, we get DAC step size = 0.5v. The comparator output will be high as long as $V_{DAC} < V_{in}$ i.e. $V_{DAC} < 6.2v$. As soon as $V_{DAC} > 6.2v$ the output of comparator will go low. Consequently, output of AND gate will be low and clock pulses will not reach to the counter and its output will remain stable. This condition will reach in the 13th step of DAC i.e. $13 \times 0.5 = 6.5v$. Therefore, the stable reading of LED display will be 13 and option 'd' is correct.

- 10.4** We've obtained the stable output of DAC $V_{DAC} = 6.5 \text{ v}$ in the previous part of this example and $V_{in} = 6.2 \text{ v}$ is given. So, the difference between their magnitude i.e. error = $6.5 - 6.2 = 0.3v$. So, option 'b' is correct.

- 10.5** It is a R-2R ladder DAC and current from voltage source = $\frac{V_R}{R} = \frac{10V}{10 \text{ k}\Omega} = 1mA$. We also know that the current gets divided in 2 equal parts at every node and there are such 4 nodes through which I reach.

$$\therefore I = \frac{\text{current from voltage source}}{2^4} = \frac{1mA}{16} = 62.5 \mu A. \quad \text{Therefore, option 'b' is correct.}$$

- 10.6** It is clear from the given figure that the current through the inverting terminal of the OPAMP is

$$I_{inv} = \frac{I}{4} + \frac{I}{16} = \frac{5}{16} I$$

$$\text{So, } V_0 = -(I_{inv} \times R) = -\frac{5 \times 10}{16} v = -3.125v \text{ i.e. option 'c'}.$$